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⑳ Method of obtaining high quality silicon dioxide passivation on silicon carbide and resulting passivated structures.

㉑ A method of obtaining high quality passivation layers on silicon carbide surfaces by oxidizing a sacrificial layer of a silicon-containing material on a silicon carbide portion of a device structure to substantially consume the sacrificial layer to produce an oxide passivation layer on the silicon carbide portion that is substantially free of dopants that would otherwise degrade the electrical integrity of the oxide layer. The oxidizing of the sacrificial layer is preferably achieved by thermal oxidizing. The silicon carbide portion may be of p-type silicon carbide which is aluminium doped.

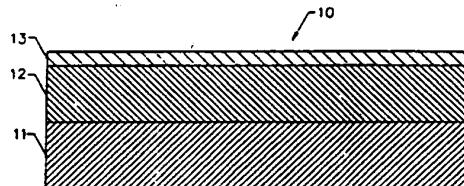


FIG. 3A.

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The present invention relates to a method of passivating microelectronic structures and in particular relates to passivation of silicon carbide structures using silicon dioxide.

Silicon carbide (SiC) has a number of theoretical and practical advantages that make its use desirable in microelectronic devices. These advantages are fairly well known and include a wide band gap, a high breakdown field, high thermal conductivity, high electron drift velocity, excellent thermal stability, and excellent radiation resistance or "hardness." These advantages have been recognized and described thoroughly in the patent and nonpatent literature.

One of the chemical advantages of silicon carbide is its ability to form a stable and well understood oxide, namely silicon dioxide (SiO_2), that can be used to passivate silicon carbide structure and devices. As known to those familiar with electronic devices, an appropriate thermally-grown oxide passivation layer provides an associated advantageous oxide-semiconductor interface that largely eliminates the presence of dangling bonds (sometimes referred to as dangling valences) on the semiconductor surface, and thus largely eliminates the associated problems such as interface charges and traps.

There are, however, some problems that arise from silicon dioxide passivation on silicon carbide because of certain properties of silicon carbide. In particular, a common p-type dopant for silicon carbide is aluminum. Although aluminum gives the highest p-type conductivity in silicon carbide, it recently has been discovered that the presence of aluminum incorporated into the thermally grown oxide passivation layers on p-type silicon carbide tend to cause high fixed oxide charge and high trap density at the silicon dioxide-silicon carbide interface. If the aluminum concentration is sufficiently high (for example when an oxide is grown on p^+ silicon carbide) the resulting oxide can have very high leakage currents, rendering it disadvantageous or even useless for passivation or electrical isolation. This problem does not occur when passivating silicon with silicon dioxide because aluminum is not a common dopant for silicon.

As a result of these characteristics, when thermally grown oxides have been used to passivate structures such as mesa p^+/n^- junctions in silicon carbide, the resulting devices tend to demonstrate excessive leakage currents in reverse bias at relatively high voltages (i.e., greater than 50 volts). This leakage current is apparently caused by the poor quality of the passivation on the p^+ side of the junction, causing what effectively amounts to a short circuit around the junction. In some p-channel MOSFETs (metal-oxide-semiconductor field effect transistor), the gate contact has been observed to

short entirely through the oxide where it overlaps the p^+ source and drain wells.

Additionally, in n-channel MOSFETs, where the electrical integrity of the oxide layers over the aluminum doped p-type channel region are extremely important, the high interface trap density and fixed oxide charge tend to cause the transistors to have high threshold voltages, low transconductances, low channel mobilities at room temperature, and all of which properties tend to change dramatically with temperature. As these MOSFETs are heated, their behavior improves because the increasing density of thermally generated carriers tend to fill the interface traps.

Another problem that arises from the difference between silicon carbide and silicon is that carbon-oxygen compounds are generated by the oxidation of silicon carbide during passivation that are not generated during passivation of silicon. Although not known for certain, these carbon-oxygen species may have their own degrading effect on the electrical integrity of silicon dioxide layers grown on silicon carbide, possibly contributing to fixed oxide charge and premature electric breakdown or wear out.

Finally, earlier work has demonstrated that n-type dopants such as nitrogen tend to pile up severely during thermal oxidation of silicon carbide, resulting in an interfacial concentration more than ten times higher than the bulk of the material. Such dopant pile up could additionally have a profound effect on the electrical characteristics of devices such as MOSFETs.

Therefore, there exists the need to develop a method for passivating silicon carbide device structures advantageously with silicon dioxide while avoiding the aforementioned problems.

The object of the present invention is to provide a method, and resulting structures, of obtaining high quality passivation layers on silicon carbide surfaces, and their associated high quality oxide-semiconductor interfaces in which the oxide passivation layers are substantially free of dopants and carbon-oxygen by-product species that would otherwise degrade the electrical integrity of the oxide layer.

The invention meets this object by oxidizing a sacrificial layer of a silicon-containing material on a silicon carbide portion of a device structure to substantially consume the sacrificial layer to produce an oxide passivation layer on the silicon carbide portion that is substantially free of dopants and of carbon-oxygen by-product species that would otherwise degrade the electrical integrity of the oxide layer.

In another embodiment, the invention comprises oxidizing a device structure formed of a layer of silicon dioxide of a desired thickness on a

silicon carbide portion of the device structure to slightly extend the interface between the silicon dioxide and the silicon carbide into the silicon carbide portion. Further to this embodiment, the method comprises depositing a layer of silicon dioxide of a desired thickness on the silicon carbide portion of the device structure without oxidizing the silicon carbide portion prior to the step of oxidizing the device structure.

In another embodiment, the invention comprises a silicon carbide based device precursor structure comprising a silicon carbide portion and a sacrificial layer of a silicon-containing material on the silicon carbide portion in which the sacrificial layer is selected from the group consisting of polycrystalline silicon (Si), silicon nitride (Si_3N_4), or undoped silicon carbide.

In another embodiment, the invention comprises a silicon carbide-based device structure having passivation areas that are substantially free of the impurities normally associated with oxides grown on silicon carbide in which the structure comprises a silicon carbide portion and a thermally grown oxidation layer on the silicon carbide portion in which the oxidation layer is substantially free of aluminum and of carbon-oxygen by-products typically associated with thermal oxidation of silicon carbide.

The foregoing and other objects, advantages and features of the invention, and the manner in which the same are accomplished, will become more readily apparent upon consideration of the following detailed description of the invention taken in conjunction with the accompanying drawings which illustrate preferred and exemplary embodiments, and wherein:

Figure 1 is a plot of drain current-voltage characteristics of a 6H-SiC inversion-mode MOSFET at (a) 298K, (b) 473K, and (c) 673K;

Figure 2 is another plot of drain current-voltage characteristics for a 6H-SiC n-channel inversion-mode MOSFET showing the effects of reducing aluminum in the oxide and measured at (a) 298K, (b) 423K, and (c) 573K;

Figures 3(a) and 3(b) are the initial and final device structures for an n-channel planar MOSFET structure incorporating the present invention; and Figures 4(a), (b), and (c) are progressive cross-sectional views of the processing methodology for a hi-lo IMPATT diode incorporating the present invention.

The present invention is a method of obtaining high quality passivation layers on silicon carbide surfaces. In one embodiment, the method comprises oxidizing a sacrificial layer of a silicon-containing material on a silicon carbide portion of a device structure to substantially consume the sacrificial layer to produce an oxide passivation layer

on the silicon carbide portion that is substantially free of dopants and carbon-oxygen byproduct species that would otherwise degrade the electrical integrity of the oxide layer. In the preferred embodiment, the method further comprises the step of forming the sacrificial layer of a silicon containing material on a silicon carbide portion of a device structure prior to the step of thermally oxidizing the sacrificial layer. In preferred embodiments, the step of forming the sacrificial layer comprises forming the sacrificial layer from the group consisting of polycrystalline silicon, silicon nitride or undoped silicon carbide. As used herein, an undoped layer of silicon carbide would preferably have a carrier concentration of $5E16$ ($5 \times 10^{-16} \text{ cm}^{-3}$) or less.

Silicon is the most preferred material for the sacrificial layer because it is free of carbon to begin with, and hence substantially eliminates the presence of carbon-oxygen byproducts when oxidized. Furthermore, silicon oxidizes much faster than silicon carbide, so that at an appropriate oxidation rate for silicon, the oxidation effectively stops when the silicon has been consumed, but before any appreciable amount of silicon carbide will be consumed. As a result, a high quality SiO_2 -SiC interface can be controllably formed.

Further to the preferred embodiment, the step of forming a sacrificial layer comprises forming a sacrificial layer of a predetermined desired thickness and wherein the step of thermally oxidizing the sacrificial layer comprises thermally oxidizing the sacrificial layer for a time sufficient to substantially consume the sacrificial layer at the rate of thermal oxidation being used.

Additionally, in preferred embodiments, the silicon carbide portion of the device structure comprises a silicon carbide portion having a polytype selected from the group consisting of the 6H, 3C, 4H, 2H and 15R polytypes of silicon carbide.

In the preferred embodiments, the step of oxidizing the sacrificial layer comprises thermally oxidizing the sacrificial layer, and most preferably while avoiding oxidation of the underlying silicon carbide portion. In this regard, the thermal oxidation should desirably produce an oxide layer having a thickness sufficient to have substantially consumed the sacrificial layer based on the thickness of the sacrificial layer and the oxide consumption factor of the silicon containing material in the sacrificial layer. As used herein, the consumption factor for the silicon-containing material's oxidation represents the ratio of the density of silicon atoms in silicon dioxide to the density of silicon atoms in the silicon-containing material. Thus, the step of thermally oxidizing the sacrificial layer comprises oxidizing the layer on the basis of the layer's thickness and the oxide consumption factor for the silicon-containing material.

As discussed in the background, the method of the invention is most useful in avoiding contamination of aluminum into the oxide. Accordingly, the step of forming a sacrificial layer preferably comprises forming the sacrificial layer on a p-type portion of silicon carbide, and most preferably on an aluminum doped p-type portion of silicon carbide.

As a further advantage, the use of the sacrificial layer of the present invention eliminates the potential for dopant redistribution in the underlying SiC during thermal oxidation, a problem that can arise when the SiC layer is oxidized directly.

In an alternative embodiment, the method can comprise the step of depositing a boron-doped silicon carbide layer between the silicon carbide portion and the sacrificial silicon layer when silicon is used as the sacrificial layer. The boron-doped silicon carbide layer can be selected from the group consisting of semi-insulating boron-doped silicon carbide layers and p-type boron-doped silicon carbide layers.

In another alternative embodiment, the sacrificial layer can be formed entirely of a boron-doped silicon carbide epitaxial layer. As known to those familiar with silicon carbide and silicon dioxide, boron (B) is a p-type dopant for silicon carbide, but one which has little or no negative effect on the electronic properties of silicon dioxide. Additionally, because such a layer has p-type characteristics, it need not be entirely consumed during oxidation when used over another p-type SiC layer or substrate.

In a preferred embodiment, when a silicon layer is used as the sacrificial layer, the method comprises oxidizing the silicon layer to produce an oxide passivation layer having an aluminum dopant concentration of 3E17 ($3 \times 10^{-17} \text{ cm}^{-3}$) or less.

In an alternative embodiment, the method of the invention can comprise oxidizing a device structure formed of a layer of silicon dioxide of a desired thickness on a silicon carbide portion of the device structure to slightly extend the interface between the silicon dioxide and the silicon carbide into the silicon carbide portion. As in the previous embodiment, the oxidizing step preferably comprises thermal oxidation of the device structure. Most preferably, the method of this embodiment further comprises the step of depositing the layer of silicon dioxide of a desired thickness on the silicon carbide portion of the device structure without oxidizing the silicon carbide portion prior to the step of oxidizing the overall device structure. In this regard, the preferred method of depositing a layer of silicon dioxide of a desired thickness on the silicon carbide portion comprises depositing the layer by chemical vapor deposition. As in the previous embodiment, the silicon carbide portion pref-

erably has a polytype selected from the group consisting of the 6H, 3C, 4H, 2H and 15R polytypes of silicon carbide. Similarly, the invention has been found to be most useful when the step of depositing the layer of silicon dioxide comprises depositing the layer on an aluminum doped, p-type portion of silicon carbide.

In another embodiment, the invention comprises a silicon carbide-based device precursor structure comprising a silicon carbide portion and a sacrificial layer of a silicon-containing material on the silicon carbide portion, with the sacrificial layer being selected from the group consisting of polycrystalline silicon, polycrystalline silicon nitride or undoped silicon carbide (polycrystalline or epitaxial). The carrier concentrations preferred for undoped silicon carbide in the previous embodiments would similarly be preferred for this embodiment. In particular, in a preferred embodiment of the device precursor structure of the invention, the sacrificial layer comprises undoped silicon carbide having a carrier concentration of 5E16 ($5 \times 10^{-16} \text{ cm}^{-3}$) or less.

In another embodiment, the invention comprises a silicon carbide base device structure having passivation areas that are substantially free of the impurities normally associated with oxides grown on silicon carbide. The structure comprises a silicon carbide portion, and a thermally grown oxidation layer upon the silicon carbide portion, the oxidation layer being substantially free of aluminum and of carbon-oxygen by-products typically associated with thermal oxidation of silicon carbide. In the most preferred device structure, the oxidation layer has an aluminum dopant concentration of 3E17 ($3 \times 10^{-17} \text{ cm}^{-3}$) or less. As known to those familiar with silicon carbide and with microelectronic device structures, the silicon carbide portion of the device structure can be selected from the group consisting of substrates, epitaxial layers, mesa sidewalls, implanted or diffused wells, and any combination of these structural elements.

Figures 1 and 2, although not representing identical devices, demonstrate some of the advantages of the present invention. Figure 1 is a set of three plots of drain current versus drain voltage at selected gate voltages for a 6H-SiC Inversion-mode MOSFET at temperatures of 298K, 473K, and 673K. The techniques of the present invention were not used in producing the MOSFET characterized by Figure 1, and Figure 1 is thus included for comparative purposes.

By way of such comparison, Figure 2 represents the same information as Figure 1 taken at 298K, 423K, and 573K in which an attempt was made to eliminate aluminum entirely from the oxide. This was first attempted on some planar MOSFETs fabricated on the Si-face of silicon carbide

and utilizing ion implanted n^+ source and drain wells. By way of further comparison, the device of Figure 1 was produced using dry oxide techniques, while that of Figure 2 was produced by a wet oxide process. Furthermore, the p-channel of the Figure 2 device contained less aluminum than the p-channel of the Figure 1 device.

Appropriate techniques for producing bulk silicon carbide, epitaxial layers of silicon carbide, ion implantation of silicon carbide, and dry etching of silicon carbide are set forth in numerous prior patents. These include U.S. Patents Nos. 4,912,063; 4,912,064; 4,865,685; 4,866,005; and 5,087,576.

The major difference between the MOSFETs formed in the attempt to eliminate aluminum from the oxide and previous MOSFETs was the incorporation of a very thin layer of undoped 6H-SiC grown on top of the p-channel layer. The p-type layer was first grown and measured to have $p = 4.3 \times 10^{15} \text{ cm}^{-3}$. Next, an epitaxial layer of undoped silicon carbide only 37 nanometers (nm) thick ($n = 2-8 \times 10^{15} \text{ cm}^{-3}$) was grown on top. As previously described herein, the purpose of including this layer is to consume it during oxidation so that the SiO_2/SiC interface stops at a point very close to the p-type material or only one or two monolayers into it.

After fabricating the devices and implanting the wells, the device wafers were oxidized in wet oxygen at 1200 °C for 49 minutes, yielding an oxide thickness of 62 nanometers. Assuming an oxide consumption factor of 0.47, and the loss of about 6 nanometers in a previous reactive ion etching (RIE) step, this thickness would have brought the SiO_2/SiC interface to within about 2 nm of the p-type material. Although it could not be specifically confirmed whether such dimensions were really the case or whether the interface had aluminum present, it was certain that there was much less aluminum present in the oxide than in previous MOSFETs.

Figures 1 and 2 show the improvements provided by the invention in such devices. For the device characterized in Figure 1, the maximum transconductance was 0.25 millisiemens per millimeter (mS/mm) at a gate voltage of +24 volts (V). The on-current at a gate voltage of +16 V was 0.5 milliamps (mA). In the invention, and as indicated in Figure 2, the room temperature drain current at a gate voltage of 16 volts was 18.6 mA and the transconductance at that gate voltage was 2.8 mS/mm. The threshold voltage was about 1.9 volts, which is much lower than the 9 to 12 volts obtained for the device in Figure 1. The channel mobility was measured to be about 46 $\text{cm}^2/\text{V}\cdot\text{sec}$, and the subthreshold leakage current (gate voltage equals 0 volts) was 560 nanoamps (nA).

Figures 2(b) and 2(c) show the comparative operation of the device at higher temperatures. When the temperature was raised to 150 °C, as shown in Figure 2(b), both the current and transconductance at a gate voltage of 16 volts increased to 29 mA and 3.6 mS/mm, and the threshold voltage decreased to about -0.2 volts. This trend continued up to 300 °C, as shown in Figure 2(c). At this temperature, the current and transconductance at the gate voltage of 16 volts were 35 mA and 3.9 mS/mm, respectively. Although the threshold voltage of the device fell to -0.8 volts, the drain current at a gate voltage of 0 volts was only 47 microamps (μA). The channel mobility at 300 °C decreased to about 43.5 $\text{cm}^2/\text{V}\cdot\text{sec}$.

Figures 3 and 4 further illustrate the use of the invention and the resulting product.

Figure 3(a) shows a device precursor broadly designated at 10 formed of an n-type 6H-SiC substrate 11 and a p-type 6H epitaxial layer 12. In accordance with the invention, and in preparation for passivation, a sacrificially undoped epitaxial layer ("epilayer") 13 is added upon the p-type epitaxial layer 12.

After oxidation and further processing the finished device, again designated at 10 for the sake of consistency, is illustrated in Figure 3(b). Figure 3(b) again illustrates the n-type substrate 11 and p-type epitaxial layer 12, but also shows respective n^+ implanted wells 14 and 15, a metallic source contact 16, a metallic drain contact 17, and a metallic gate contact 18. In preferred embodiments, the source and drain contacts 16,17 are formed of nickel and the gate contact 18 of molybdenum. The oxide layer 19 resulting from the oxidation of the undoped epitaxial layer 13, is also illustrated in Figure 3(a). By incorporating the method of the present invention, the oxide layer 19 is formed from the undoped layer 13 rather than from the p-type layer 12 to thus minimize the dopant concentration in the oxide and any associated problems.

Figure 4 shows the progressive formation of a mesa type IMPATT (impact avalanche transit time) device broadly designated at 20 and incorporating the method of the present invention. Figure 4(a) illustrates an n-type 6H SiC substrate 21, an n-type epilayer 22, a second n-type epilayer 23, and a p-type epilayer 24. In a typical embodiment, the first n-type epitaxial layer 22 has a carrier concentration of between about 2 and 3E16, the second n-type epitaxial layer 23 has a carrier concentration of about 7E17, and the p-type epitaxial layer has a carrier concentration of 5E18 or higher.

Figure 4(b) illustrates the same structure but with the addition of a thin layer of polysilicon 25 to both the mesa and rear portions of the device. The thin polysilicon layer 25 is, of course, the sacrificial

layer referred to herein. As set forth earlier herein, in certain embodiments a thin boron-doped silicon carbide layer can be added between the polysilicon layer 25 and the surface or edges of the respective SiC layers 21, 22, 23 and 24. The boron-doped layer should be thick enough to keep aluminum from the interface while otherwise remaining as thin as possible. An appropriate thickness presently appears to be between about 1 and 50 nm.

Figure 4(c) illustrates a completed device after incorporation of the invention. The difference from Figure 4(b) is the consumption of the polysilicon layer on the mesa portion of the device to form the passivation oxide layer 26. Again, by incorporating the invention, the dopant concentration in the oxide layer 26 can be kept very low, particularly adjacent the heavily doped p-type epitaxial layer 24. As set forth earlier, if the oxide layer 26 had a sufficient carrier concentration, a short circuit could occur between layers 24 and 23, thus incapacitating the device.

To complete the device, Figure 4 also illustrates an ohmic contact 27 to the substrate, preferably formed of nickel, and an ohmic contact 28 to the p-type epitaxial layer on the mesa, and preferably formed of an aluminum alloy.

It will be understood to those familiar with such devices that the invention can also be applied to structures in addition to those illustrated herein, including p-channel planar MOSFETs having implanted p-type wells, and those in which the p-type source and drain are formed from epilayers that have been partially etched away. In either case, an oxide typically will border both a p-portion and an n-portion of the device so that any leakage through the oxide portion will essentially short the device, the avoidance of which is one of the main advantages of the present invention.

The invention can also be applied to any vertical power MOSFET design in SiC, such as DDMOS (double diffused MOS), UMOS (U-channel MOS), or VMOS (V-channel MOS), that would require use of aluminum as the channel dopant.

In the drawings and specifications, there have been disclosed typical preferred embodiments of the invention and, although specific terms have been employed, they have been used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.

Claims

1. A method of obtaining high quality passivation layers on silicon carbide surfaces, the method being characterised by:
oxidizing a sacrificial layer of a silicon-containing material on a silicon carbide portion

5 of a device structure to substantially consume the sacrificial layer to produce an oxide passivation layer on the silicon carbide portion that is substantially free of dopants and other species that would otherwise degrade the electrical integrity of the oxide layer.

2. A method according to claim 1 and further characterized by the step of forming the sacrificial layer of a silicon-containing material on a silicon carbide portion of a device structure prior to the step of thermally oxidizing the sacrificial layer.
3. A method according to claim 1 or 2 characterised in that the step of oxidizing the sacrificial layer comprises thermally oxidizing the sacrificial layer.
4. A method according to claim 1, 2 or 3, characterised in that the step of forming a sacrificial layer of a silicon-containing material comprises forming the sacrificial layer from the group consisting of: polycrystalline silicon, silicon nitride, boron-doped silicon carbide, or undoped silicon carbide.
5. A method according to any preceding claim, characterised in that the step of forming a sacrificial layer of a silicon-containing material comprises forming the sacrificial layer from a silicon-containing material having an impurity concentration of impurities that can affect the electrical characteristics of the resulting oxide of $5E16$ ($5 \times 10^{16} \text{ cm}^{-3}$) or less.
6. A method according to any preceding claim characterised in that the step of forming a sacrificial layer of a silicon-containing material comprises forming the sacrificial layer from a silicon-containing material having an aluminum concentration of $5E16$ ($5 \times 10^{16} \text{ cm}^{-3}$) or less.
7. A method according to claim 3 characterised in that the step of thermally oxidising the sacrificial layer to substantially consume the sacrificial layer comprises thermally oxidizing the sacrificial layer while avoiding oxidation of the underlying silicon carbide portion.
8. A method according to claim 3 characterised in that the step of forming a sacrificial layer of a silicon-containing material comprises forming a sacrificial layer of a predetermined desired thickness; and wherein
the step of thermally oxidizing the sacrificial layer to substantially consume the sacrificial

cial layer comprises thermally oxidizing the sacrificial layer for a time sufficient to substantially consume the sacrificial layer at the rate of thermal oxidation being used.

9. A method according to any preceding claim characterised in that the step of forming a sacrificial layer of a silicon-containing material on a silicon carbide portion of a device structure comprises forming the sacrificial layer on a silicon carbide portion having a polytype selected from the group consisting of: the 6H, 3C, 4H, 2H, and 15R polytypes of silicon carbide.

10. A method according to claim 3 characterised in that the step of thermally oxidizing the sacrificial layer to substantially consume the sacrificial layer comprises thermally oxidizing the sacrificial layer to produce an oxide layer having a thickness sufficient to have substantially consumed the sacrificial layer based upon the thickness of the sacrificial layer and the oxide consumption factor of the silicon-containing material in the sacrificial layer.

11. A method according to claim 10 characterised in that the sacrificial layer comprises silicon carbide and the step of thermally oxidizing the sacrificial layer comprises oxidising the sacrificial layer on the basis of thickness of the sacrificial layer and the oxide consumption factor for silicon carbide.

12. A method according to claim 11 characterised in that the consumption factor for silicon carbide is the ratio of the density of silicon atoms in silicon dioxide to the density of silicon atoms in silicon carbide.

13. A method according to any preceding claim characterised in that the step of forming a sacrificial layer of a silicon-containing material on a silicon carbide portion of a device structure comprises forming the sacrificial layer on a p-type portion of silicon carbide.

14. A method according to claim 13 characterised in that the step of forming the sacrificial layer on a p-type portion of silicon carbide comprises forming the sacrificial layer on an aluminum-doped p-type portion of silicon carbide.

15. A method according to any preceding claim characterised in that the step of oxidizing the sacrificial layer comprises:

oxidizing a device structure formed of a layer of silicon dioxide of a desired thickness

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16. A method according to claim 15 characterised in that it further comprising the step of depositing a layer of silicon dioxide of a desired thickness on the silicon carbide portion of the device structure and without oxidizing the silicon carbide portion prior to the step of oxidizing the device structure.

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17. A method according to claim 16 characterised in that the step of depositing a layer of silicon dioxide of a desired thickness on a silicon carbide portion of a device structure comprises depositing the layer by chemical vapor deposition.

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18. A method according to claim 1 characterised in that the sacrificial layer is formed of silicon, and further comprising the step of depositing a thin boron-doped silicon carbide epitaxial layer between the silicon carbide portion and the sacrificial silicon layer and in which the layer is thick enough to prevent aluminum from reaching the resulting oxide while otherwise remaining as thin as possible.

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19. A method according to claim 18 characterised in that the step of depositing a boron-doped silicon carbide epitaxial layer comprises depositing a layer selected from the group consisting of: semi-insulating boron-doped silicon carbide layers and p-type boron-doped silicon carbide layers.

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20. A method according to claim 8 or 9, characterised in that the step of thermally oxidizing the silicon layer comprises oxidizing the silicon layer to produce an oxide passivation layer on the silicon carbide portion in which the oxide layer has an aluminum dopant concentration of $3E17 (3 \times 10^{-17} \text{ cm}^{-3})$ or less.

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21. A silicon carbide-based device structure having passivation areas that are substantially free of the impurities normally associated with oxides grown on doped silicon carbide, said structure comprising:

a silicon carbide portion; and

a thermally-grown oxidation layer upon said silicon carbide portion, said oxidation layer being substantially free of aluminum.

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22. A device structure according to claim 21 characterised in that said oxidation layer has

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an aluminum dopant concentration of 3E17 (3
 $\times 10^{-17}$ cm⁻³) or less.

23. A device according to claim 21 or 22 characterised in that said silicon carbide portion is selected from the group consisting of: substrates, epitaxial layers, mesa sidewalls, implanted or diffused wells and any combinations thereof.

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24. A device structure according to claim 21, 22 or 23 characterised in that said oxidation layer is substantially free of carbon-oxygen by-products typically associated with thermal oxidation of silicon carbide.

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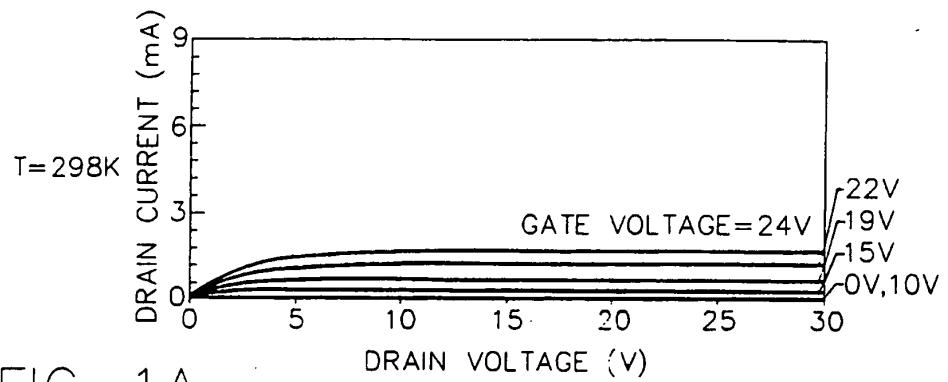


FIG. 1A.

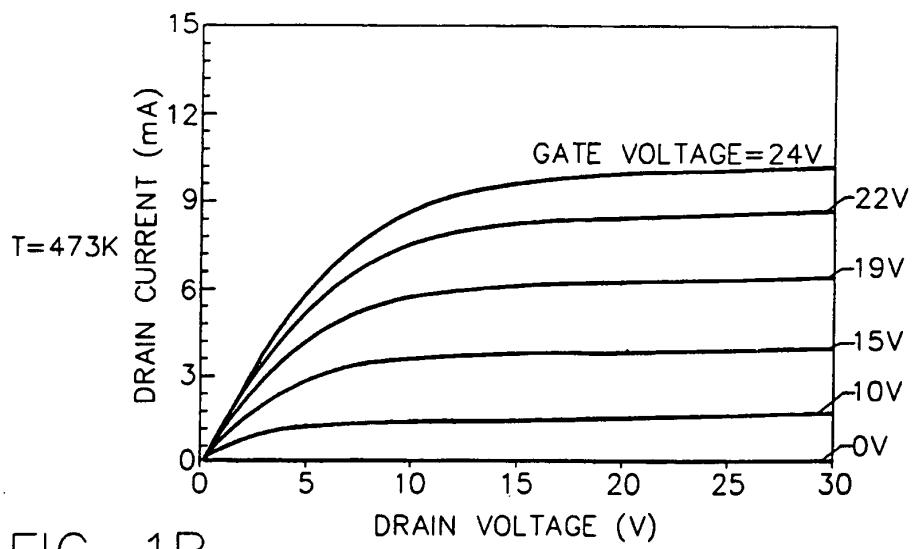


FIG. 1B.

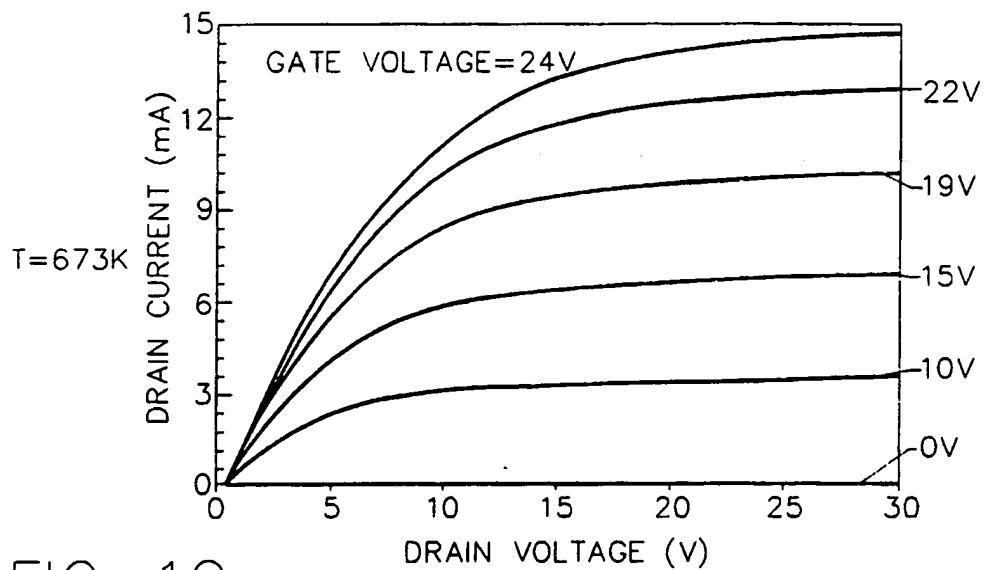


FIG. 1C.

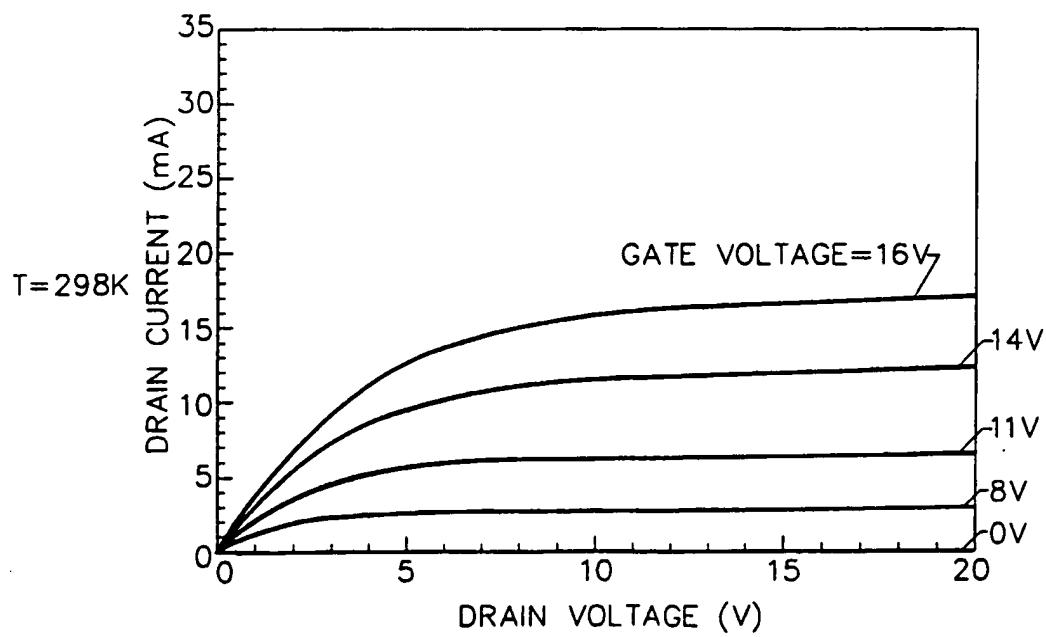


FIG. 2A.

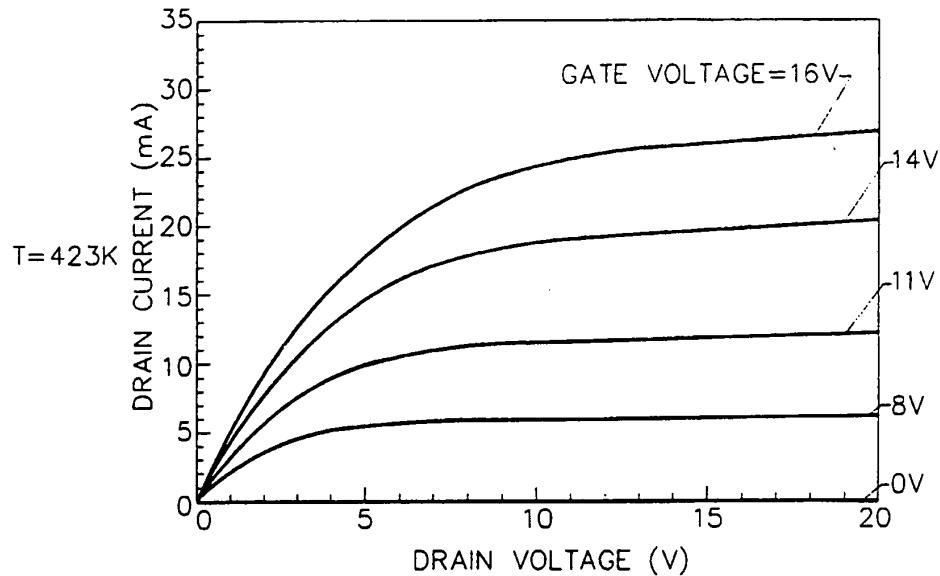


FIG. 2B.

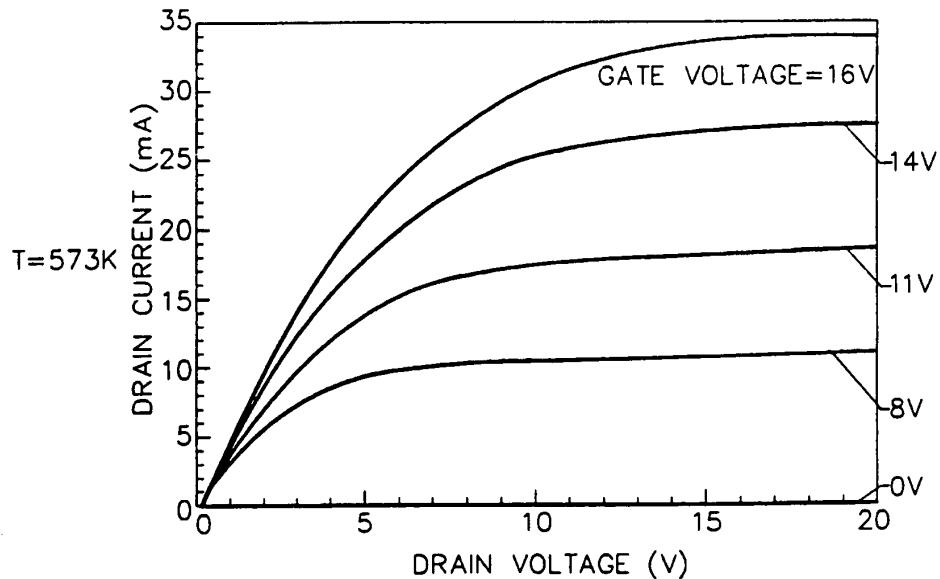


FIG. 2C.

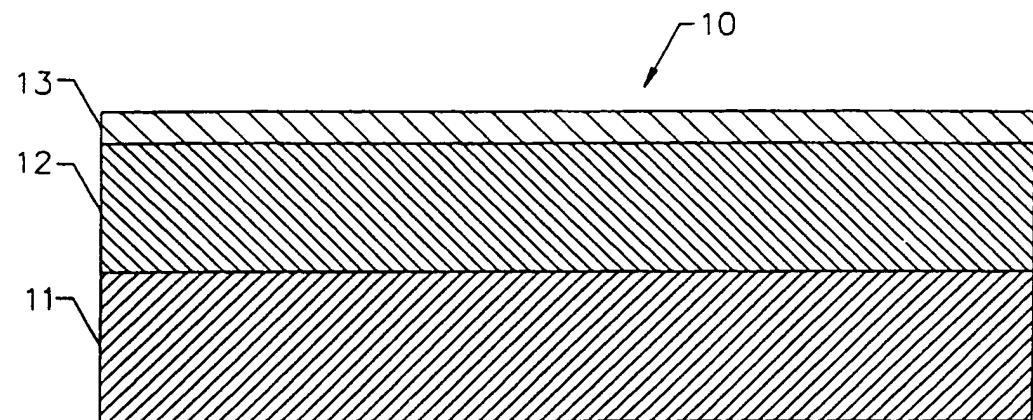


FIG. 3A.

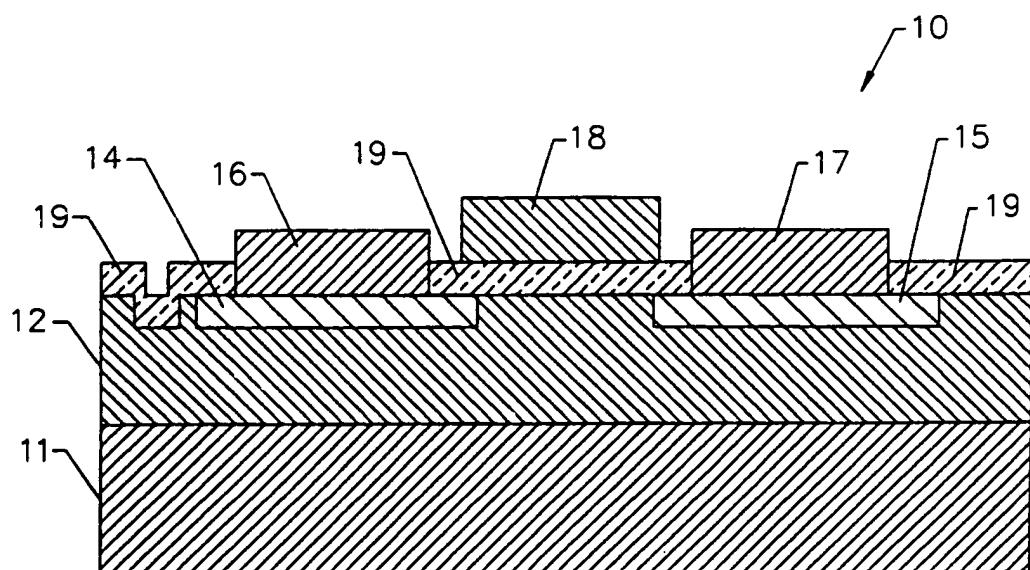


FIG. 3B.

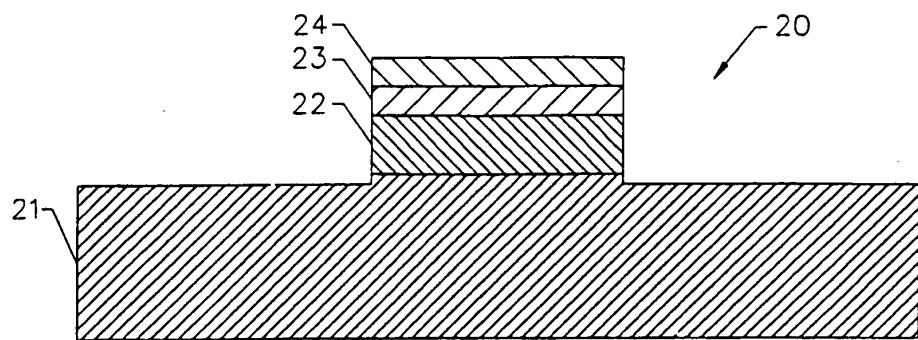


FIG. 4A.

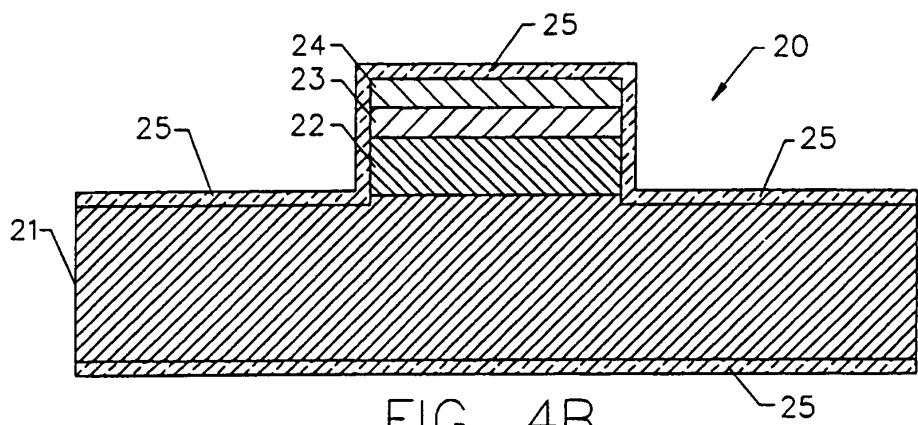


FIG. 4B.

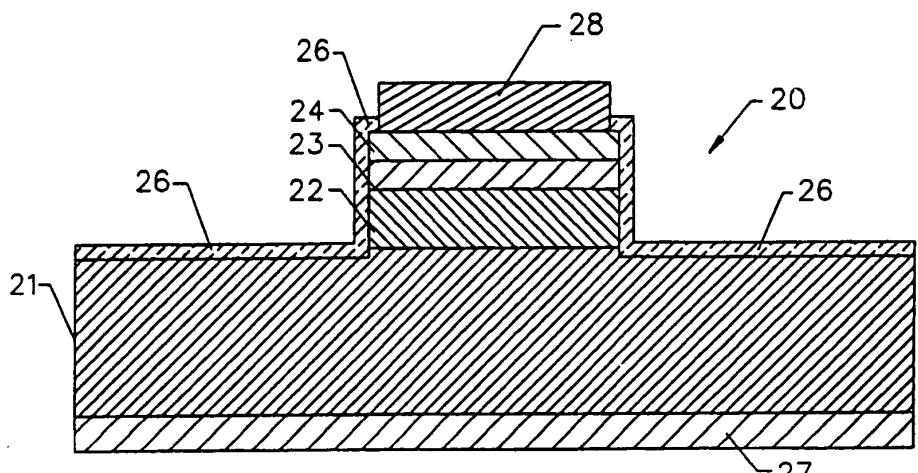


FIG. 4C.



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EUROPEAN SEARCH REPORT

Application Number
EP 93 30 6024

DOCUMENTS CONSIDERED TO BE RELEVANT			CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	
X	DE-A-34 34 727 (SHARP) * page 5, line 19 - page 6, line 18 * ---	1-5,7-9	H01L21/473 H01L29/24
X	EP-A-0 363 944 (FUJITSU) * claim 1; figure 2 * ---	1-4,6-9, 21,23	
A	DE-A-40 09 837 (SHARP) * abstract; figure 2 * ---	1,21	
A	JOURNAL OF THE ELECTROCHEMICAL SOCIETY vol. 136, no. 2, February 1989, MANCHESTER, NEW HAMPSHIRE US pages 502 - 507 PALMOUR ET AL 'Dopant redistribution during thermal oxidation of monocrystalline Beta-SiC thin films' * abstract * -----	1,21	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
			H01L
<p>The present search report has been drawn up for all claims</p>			
Place of search	Date of completion of the search	Examiner	
THE HAGUE	4 January 1994	Gori, P	
CATEGORY OF CITED DOCUMENTS			
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons A : member of the same patent family, corresponding document	